1. ADD(R)

|  |
| --- |
| PC → Mem\_a/ alu1\_a  Mem\_d → ir  +1 → alu1\_b  alu1\_out → PC |
|
|
|
|
| ir9-11 → rf\_a1  ir6-8 →rf\_a2  rf\_d1 → t1  rf\_d2 → t2 |
|
|
|
|
| t1 → alu2\_a  t2 → alu2\_b  alu2\_out →t1 |
|
|
|
|
|
|
| t1 → rf\_d3  ir3-5 → rf\_a3  if(rf\_a3 == R7){  t1->PC  }  else{  PC-> R7} |
|
|
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|
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1. ADC(R)

|  |
| --- |
| PC → Mem\_a/ alu1\_a  Mem\_d → ir  +1 → alu1\_b  alu1\_out → PC |
|
|
|
|
| ir9-11 → rf\_a1  ir6-8 →rf\_a2  rf\_d1 → t1  rf\_d2 → t2  If (C flag==0 & OPCODE) then PC -> R7 |
|
|
|
|
| if(C==1){enable t1, CZ}  else (disable the t1, CZ)  t1 → alu2\_a  t2 → alu2\_b  alu2\_out →t1 |
|
|
|
|
| t1 → rf\_d3  ir3-5 → rf\_a3  if(rf\_a3 == R7){  t1->PC  }  else{  PC-> R7} |
|
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1. ADZ(R)

|  |
| --- |
| PC → Mem\_a/ alu1\_a  Mem\_d → ir  +1 → alu1\_b  alu1\_out → PC |
|
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|
|
| ir9-11 → rf\_a1  ir6-8 →rf\_a2  rf\_d1 → t1  rf\_d2 → t2  If (Z flag==0 & OPCODE) then PC -> R7 |
|
|
|
|
| if(Z==1){enable t1, CZ}  else (disable the t1, CZ)  t1 → alu2\_a  t2 → alu2\_b  alu2\_out →t1 |
|
|
|
|
| t1 → rf\_d3  ir3-5 → rf\_a3  if(rf\_a3 == R7){  t1->PC  }  else{  PC-> R7} |
|
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|
|

1. ADI (I)

|  |
| --- |
| PC → Mem\_a/ alu1\_a  Mem\_d → ir  +1 → alu1\_b  alu1\_out → PC |
|
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|
|
| ir9-11 → rf\_a1  ir6-8 →rf\_a2  rf\_d1 → t1  rf\_d2 → t2 |
|
|
|
|
| t1 → alu2\_a  ir0-5 → SE6 → alu2\_b  alu2\_out →t1 |
|
|
|
|
| t1 → rf\_d3  ir6-8 → rf\_a3  if(rf\_a3 == R7){  t1->PC  }  else{  PC-> R7} |
|
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1. NDU
2. NDC
3. NDZ
4. LHI (J)

|  |
| --- |
| PC → Mem\_a/ alu1\_a  Mem\_d → ir  +1 → alu1\_b  alu1\_out → PC |
|
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|
| ir9-11 → rf\_a1  ir6-8 →rf\_a2  rf\_d1 → t1  rf\_d2 → t2 |
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|
| ir0-8 → LSHIFT-7→ t2 |
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|
|
| ir0-8 → LSHIFT-7 → rf\_d3  ir9-11 → rf\_a3  if(rf\_a3 == R7){  ir0-8 → LSHIFT-7->PC  }  else{  PC-> R7} |
|
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1. LW (I)

|  |
| --- |
| PC → Mem\_a/ alu1\_a  Mem\_d → ir  +1 → alu1\_b  alu1\_out → PC |
|
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|
|
| ir9-11 → rf\_a1  ir6-8 →rf\_a2  rf\_d1 → t1  rf\_d2 → t2 |
|
|
|
|
| ir0-5 → SE6→ alu2\_B  t2 → alu2\_a  alu2\_out → t1 |
|
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|
| t1 → Mem\_a  Mem\_d → t1 |
|
|
|
|
| t1 → alu2\_a, rf\_d3  0 → alu\_b  ir9-11 → rf\_a3  if(rf\_a3 == R7){  t1->PC  }  else{  PC-> R7} |
|
|
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1. SW

|  |
| --- |
| PC → Mem\_a/ alu1\_a  Mem\_d → ir  +1 → alu1\_b  alu1\_out → PC |
|
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|
|
| ir9-11 → rf\_a1  ir6-8 →rf\_a2  rf\_d1 → t1  rf\_d2 → t2 |
|
|
|
|
| ir0-5 → SE6→ alu2\_b  t2 → alu2\_a  alu2\_out → t2 |
|
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|
|
| t1 → Mem\_d  t2 → Mem\_a  111 → rf\_a3  PC → R7 |
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|

1. LM

|  |
| --- |
| PC → Mem\_a/ alu1\_a  Mem\_d → ir  +1 → alu1\_b  alu1\_out → PC |
|
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|
| ir9-11 → rf\_a1  ir6-8 →rf\_a2  rf\_d1 → t1  rf\_d2 → t2 |
|
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|
| ir0-8 → SE9 → t2 |
|
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|
|
| t2 → PE (PE clears least significant 1 of t2)  PE -> t2  PE\_addr → t4 (3 bit)  t1 → Mem\_a  Mem\_d → t3 |
|
|
|
|
| t4 → rf\_a3  t3 → rf\_d3  t1 → alu1\_a  +1 → alu1\_b  alu1\_out → t1  if(rf\_a3 == R7){  t3->PC  }  else{  PC-> R7} |
|
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1. SM

|  |
| --- |
| PC → Mem\_a/ alu1\_a  Mem\_d → ir  +1 → alu1\_b  alu1\_out → PC |
|
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|
|
| ir9-11 → rf\_a1  ir6-8 →rf\_a2  rf\_d1 → t1  rf\_d2 → t2 |
|
|
|
|
| ir0-8 → SE9 → t2 |
|
|
|
|
| t2 → PE (PE clears least significant 1 of t2)  PE\_addr → t4 (3 bit) |
|
|
|
|
| t4 → rf\_a1  rf\_d1 → t3 |
|
|
|
|
| t1 → Mem\_a  t3 → Mem\_d  t1 → alu1\_a  +1 → alu1\_b  alu1\_out → t1  PC -> R7 |
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1. BEQ

|  |
| --- |
| PC → Mem\_a/ alu1\_a  Mem\_d → ir  +1 → alu1\_b  alu1\_out → PC |
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|
|
| ir9-11 → rf\_a1  ir6-8 →rf\_a2  rf\_d1 → t1  rf\_d2 → t2 |
|
|
|
|
| t1 → alu2\_a  t2 → alu2\_b  111 → rf\_a1  rf\_d1 → t1 |
|
|
|
| if (tempz==0){  PC -> R7  }  else{  t1 → alu2\_a  ir0-8 → SE9 → alu2\_b  alu\_out → PC,R7  }  else{  t1 → t2  } |
|
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1. JAL

|  |
| --- |
| PC → Mem\_a/ alu1\_a  Mem\_d → ir  +1 → alu1\_b  alu1\_out → PC |
|
|
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|
| ir9-11 → rf\_a1  ir6-8 →rf\_a2  rf\_d1 → t1  rf\_d2 → t2 |
|
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|
|
| 111 → rf\_a1  rf\_d1 → t3 |
|
|
|
|
| ir0-8 → SE9 → alu2\_a  t3 → alu2\_b, rf\_d3  alu\_out → PC,R7  ir9-11 → rf\_a3 |
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1. JLR

|  |
| --- |
| PC → Mem\_a/ alu1\_a  Mem\_d → ir  +1 → alu1\_b  alu1\_out → PC |
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|
| ir9-11 → rf\_a1  ir6-8 →rf\_a2  rf\_d1 → t1  rf\_d2 → t2 |
|
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|
|
| 111 → rf\_a1  rf\_d1 → t3 |
|
|
|
|
| t3 → rf\_d3  t2 → PC,R7  ir9-11 → rf\_a3 |
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